

1 Attorney Docket No. 83342

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3 APPARATUS AND METHOD FOR CALIBRATING VOLTAGE SPIKE WAVEFORMS
4 FOR THREE-PHASE ELECTRICAL DEVICES AND SYSTEMS

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6 STATEMENT OF GOVERNMENT INTEREST

7 The invention described herein may be manufactured and
8 used by or for the Government of the United States of
9 America for governmental purposes without the payment of any
10 royalties thereon or therefor.

11

12 CROSS-REFERENCE TO RELATED PATENT APPLICATIONS

13 This patent application is co-pending with one related
14 patent applications entitled APPARATUS AND METHOD FOR
15 CALIBRATING VOLTAGE SPIKE WAVEFORMS (Attorney Docket No.
16 83343), by the same inventor as this application.

17

18 BACKGROUND OF THE INVENTION

19 (1) Field of the Invention

20 The present invention generally relates to an apparatus
21 and method for calibrating voltage spike waveforms that are
22 used to test survivability and compatibility of three-phase
23 electrical devices and systems.

1 (2) Description of the Prior Art

2 Many military and commercial-off-the-shelf ("COTS")
3 three-phase electrical devices have specifications that are
4 incomplete with regard to compatibility and survivability.
5 This problem is exacerbated when these electrical devices
6 are integrated with devices configured in accordance with
7 military specifications such as onboard electronics on a
8 submarine or other naval vessels. Vendors typically do not
9 perform tests or evaluations on the compatibility and
10 survivability characteristics of COTS electrical devices.
11 Typical current methodologies and schemes for testing
12 electrical devices and voltage spike suppression are
13 described in Peterson U.S. Patent No. 4,307,342, Grace et
14 al. U.S. Patent No. 5,463,315, Merritt U.S. Patent No.
15 5,525,926, Maytum U.S. Patent No. 5,623,215 and Sink U.S.
16 Patent No. 6,088,209. However, these methodologies and
17 schemes do not provide efficient techniques for testing the
18 compatibility and survivability characteristics of three-
19 phase electrical devices. Thus, what is needed is an
20 apparatus and method that can efficiently and inexpensively
21 test the compatibility and survivability characteristics of
22 three-phase electrical devices and systems.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an apparatus and method for calibrating voltage spike waveforms that are used to test the survivability and compatibility characteristics of three-phase electrical devices and systems.

It is another object of the present invention that the aforesaid apparatus and method be relatively inexpensive to implement.

Other objects and advantages of the present invention will be apparent from the ensuing description.

Thus, the present invention is directed to, in one aspect, an apparatus for calibrating voltage spikes used in testing electrical devices, comprising a circuit having a plurality of phase voltage lines and a ground line, a plurality of phase voltage inputs and a ground input adapted for connection to a power source. Each phase voltage input is connected to a corresponding phase voltage line and the ground input is connected to the ground line. The circuit further comprises a plurality of phase voltage outputs and a ground output adapted for connection to an electrical device under test. Each phase voltage output is connected to a corresponding phase voltage line and the ground output is connected to the ground line. The apparatus further comprises a selection circuit for selecting one of the phase

1 voltage lines and for providing a synchronization voltage
2 signal based on voltage signals across the phase voltage
3 lines not selected by the selection circuit, a voltage spike
4 generator for generating a predetermined voltage spike
5 waveform based on the synchronization voltage signal, and
6 additional circuitry for applying the predetermined voltage
7 spike waveform across the selected phase voltage line and
8 the ground line.

9 In a related aspect, the present invention is directed
10 to a method for calibrating voltage spikes used in testing
11 electrical devices, comprising providing a three-phase
12 electrical device to be tested, providing a three-phase
13 power source, providing a circuit having a plurality of
14 phase voltage lines and a ground line, connecting the phase
15 voltage lines between the three phase power source and the
16 electrical device under test, selecting one of the phase
17 voltage lines, generating a synchronization voltage signal
18 based on the voltage signal across the phase voltage lines
19 not selected, generating a voltage spike waveform based on
20 the synchronization voltage signal wherein the voltage spike
21 waveform has variable waveform characteristics, and applying
22 the voltage spike waveform across the selected phase voltage
23 line and the ground line. The waveform characteristics of
24 the voltage spike waveform can be varied to conform to

1 specific testing requirements for testing the electrical
2 device under test.

3

4 BRIEF DESCRIPTION OF THE DRAWINGS

5 The foregoing features of the present invention will
6 become more readily apparent and may be understood by
7 referring to the following detailed description of an
8 illustrative embodiment of the present invention, taken in
9 conjunction with the accompanying drawings, in which:

10 FIG. 1 is a block diagram showing a testing system that
11 utilizes the calibrator apparatus of the present invention;

12 FIG. 2 is a schematic diagram of the calibrator apparatus
13 of the present invention; and

14 FIG. 3 is a schematic diagram of one phase of the three
15 phase capacitor network shown in FIG. 2.

16

17 DESCRIPTION OF THE PREFERRED EMBODIMENTS

18 The present invention is directed to a three-phase
19 voltage spike waveform calibrator for implementing voltage
20 spike tests on three-phase electrical devices and equipment
21 under test. Referring to FIG. 1, there is shown a testing
22 system that utilizes voltage spike calibrator apparatus 8 of
23 the present invention. Calibrator apparatus 8 generally
24 comprises calibrator 10, voltage spike generator ("VSG") 20,
25 and synchronization circuit 25. Calibrator 10 receives and

1 calibrates voltage spikes and outputted by VSG 20. The
2 voltage spikes outputted by VSG 20 are based on
3 synchronization voltage signals provided by synchronization
4 circuit 25. The testing system shown in FIG. 1 is used to
5 perform particular tests on the unit under test ("UUT") 30
6 wherein each test requires inputting a predetermined voltage
7 spike waveform into UUT 30. UUT 30 can be any type of
8 three-phase electrical device or system. UUT 30 includes
9 phase A voltage input 40, phase B voltage input 42, and
10 phase C voltage input 44, and ground input 46. Calibrator
11 10 transforms the voltage spike outputted by VSG 20 into
12 particular voltage spike waveforms that are applied to
13 inputs 40, 42, 44 and 46 of UUT 30 in order to test the
14 survivability and compatibility of UUT 30. This feature of
15 the invention is described in detail in the ensuing
16 description.

17 Referring to FIG. 1, power supply 50 provides a supply
18 voltage and current to the UUT 30. Power supply 50 is
19 configured to provide a three-phase output and includes
20 phase A voltage output 60, phase B voltage output 62, phase
21 C voltage output 64 and ground output 66 that are inputted
22 into voltage spike attenuator 70. In a preferred
23 embodiment, power supply 50 is configured to provide 115 V_{rms}
24 and 440 V_{rms} in order to test UUT 30 with either voltage. In
25 one embodiment, VSG 20 is configured to output a voltage

1 spike having a magnitude of about 1000 volts when UUT 30 is
2 a 115 V_{rms} device, and a magnitude of about 2500 volts when
3 UUT 30 is a 440 V_{rms} device.

4 Referring to FIG. 1, voltage spike attenuator 70 is
5 connected between power supply 50 and calibrator 10 and
6 prevents high voltage spikes from being inputted into power
7 supply 50. Voltage spike attenuator 70 includes phase A
8 voltage line 80, phase B voltage line 82, phase C voltage
9 line 84, and ground line 86 that are connected to
10 corresponding phase A, phase B, and phase C voltage lines
11 and the ground input, respectively, of calibrator 10.
12 Voltage spike attenuator 70 is configured to attenuate the
13 high frequency components of the voltage spike outputted by
14 VSG 20. For example, attenuator 70 is configured to
15 attenuate a voltage spike having a peak voltage of 1000
16 volts for a 115 V_{rms} three-phase system so as to yield a
17 voltage spike having a peak voltage of 300 volts.
18 Attenuator 70 is further configured to attenuate a voltage
19 spike having a peak voltage of 2500 volts for a 440 V_{rms}
20 three-phase system so as to yield a 700 volts voltage spike.
21 Voltage spike attenuator 70 is well known in the art and is
22 therefore not discussed in detail.

23 Referring to FIG. 1, calibrator 10 includes phase A
24 voltage input 101, phase B voltage input 102, phase C
25 voltage input 104, and ground input 106 that are connected

1 to phase A voltage line 80, phase B voltage line 82, phase C
2 voltage line 84, and ground line 86, respectively, of
3 voltage spike attenuator 70. Calibrator 10 further
4 comprises phase A voltage output 116, phase B voltage output
5 118, phase C voltage output 120 and ground line 128. Phase
6 A voltage output 116, phase B voltage output 118, phase C
7 voltage output 120 and ground line 128 are connected to
8 phase A voltage input 40, phase B voltage input 42, phase C
9 voltage input 44 and ground line 46, respectively, of UUT
10 30.

11 Referring to FIG. 2, calibrator 10 comprises phase A
12 voltage line 108, phase B voltage line 110, phase C voltage
13 line 112 and ground line 114. Phase A voltage input 101 and
14 phase A voltage output 116 are connected to phase A voltage
15 line 108. Phase B voltage input 102 and phase B voltage
16 output 118 are connected to phase B voltage line 110. Phase
17 C voltage input 104 and phase voltage output 120 are
18 connected to phase C voltage line 112. Ground input 106 and
19 ground output 128 are connected to ground line 114. Fuses
20 121 provide overload protection.

21 Referring to FIG. 2, calibrator 10 further comprises
22 resistors R1, R2, R3, R4, R5 and R6 that form voltage
23 divider circuits. In one embodiment, each resistor R2, R4
24 and R6 has a resistance of about 1 K Ω , and each resistor
25 has R1, R3 and R5 has a resistance of about 99 K Ω . Each

1 capacitor C1, C2 and C3 filters out high frequencies and in
2 one embodiment, has a capacitance of about 27 pF
3 (picoFarads). However, it is to be understood that other
4 suitable resistances and capacitance values may be used.
5 Calibrator 10 further includes voltage monitoring outputs
6 122, 124 and 126. Output 122 allows measurements of voltage
7 spikes between the phase A voltage and the phase B voltage.
8 Output 124 allows for measurement of voltage spikes between
9 the phase B voltage and the phase C voltage. Similarly,
10 output 126 allows for measurement of voltage spikes between
11 the phase A voltage and the phase C voltage.

12 Referring to FIGS. 1 and 2, calibrator 10 and voltage
13 synchronization circuit 25 each comprise a portion of switch
14 130. Switch 130 comprises a plurality of groups of switch
15 contacts 130a, 130b, 130c, 130d, 130e and 130f. Voltage
16 synchronization circuit 25 comprises group 130a of switch
17 contacts. Group 130a comprises switch contacts 140, 141,
18 142, 143, 144, 145, 146 and 147. Contacts 140 and 141 are
19 inputted into switch 300 which is described in the ensuing
20 description. Switch contact 142 is connected to switch
21 contact 147 and phase B voltage line 110. Switch contact
22 143 is connected to switch contact 145 and phase C voltage
23 line 112. Switch contact 144 is connected switch contact
24 146 and phase A voltage line 108.

1 Referring to FIG. 2, calibrator 10 comprises groups
2 130b, 130c, 130d, 130e and 130f of switch contacts. Group
3 130b comprises switch contacts 150, 151, 152 and 153.
4 Switch contact 151 is connected to an open circuit. Switch
5 contacts 152 and 153 are connected to phase A voltage line
6 108. Group 130c comprises switch contacts 160, 161, 162 and
7 163. Switch contacts 161 and 163 are connected to phase B
8 voltage line 110. Switch contact 162 is connected to an
9 open circuit. Group 130d comprises switch contacts 170,
10 171, 172 and 173. Switch contacts 171 and 172 are connected
11 to phase C voltage line 112. Switch contact 173 is
12 connected to an open circuit. Group 130e comprises switch
13 contacts 180, 181, 182 and 183. Switch contact 180 is
14 connected at the junction of resistors R7 and R8. Switch
15 contact 181 is connected to phase A voltage line 108.
16 Switch contact 182 is connected to phase B voltage line 110.
17 Switch contact 183 is connected to phase C voltage line 112.
18 Group 130f comprises switch contacts 190, 191, 192 and 193.
19 Switch contact 191 is connected to switch contact 150.
20 Switch contact 192 is connected to switch contact 160.
21 Switch contact 193 is connected to switch contact 170.

22 Referring to FIGS. 2 and 3, calibrator 10 further
23 includes capacitor circuit 200 which comprises a plurality
24 of capacitor networks 202, 204, 206 and multi-level switch
25 207. Capacitor network 202 is connected between switch

1 contact 170 and ground line 114. Capacitor network 204 is
2 connected between switch contact 160 and ground line 114.
3 Capacitor network 206 is connected between switch contact
4 150 and ground line 114. Switch 207 simultaneously adjusts
5 all capacitor networks 202, 204, 206 so that each capacitor
6 network 202, 204 and 206 exhibits the same capacitance.
7 Switch 207 is adjusted so that the actual capacitance
8 exhibited by each capacitor network 202, 204 and 206
9 conforms to the particular testing requirements for UUT 30.
10 In one embodiment, switch 207 is configured as a multi-deck
11 rotary switch. However, other suitable switches can be used
12 as well. Each capacitor network 202, 204 and 206 has the
13 same circuit configuration which is shown in FIG. 3. For
14 purposes of simplicity, only capacitor network 202 is
15 described in the ensuing description. Referring to FIG. 3,
16 capacitor network 202 includes nodes 208 and 209. Node 208
17 is connected to switch contacts 170 and 193. Capacitor
18 network 204 includes nodes 209 and 210. Node 210 is
19 connected to switch contacts 160 and 192. Capacitor network
20 206 includes nodes 211 and 209. Node 211 is connected to
21 switch contacts 150 and 191. Node 209 is connected to
22 ground line 114. Switch 207 comprises a plurality of groups
23 of switch contacts. One of these groups of switch contacts
24 comprises switch contacts 210 through 217. Another group of
25 switch contacts comprises switch contacts 218 through 225.

1 A further group of switch contacts comprises switch contacts
2 226 through 233. Switch contacts 212, 214 and 216 are open
3 circuits. Switch contacts 219, 222, and 223 are also open
4 circuits. Similarly, switch contacts 227-229 are open
5 circuits. Capacitor network 202 comprises capacitors C4,
6 C5, and C6. Switch 207 can be adjusted to produce a
7 resultant capacitance between nodes 208 and 209 that is
8 based on any one of capacitors C4, C5, and C6 by themselves
9 or in any combination with each other. Thus, the resulting
10 capacitance exhibited by capacitor network 202 can be any
11 one of seven possible capacitances depending upon the
12 setting of switch 207. The seven possible resulting
13 capacitances are shown in Table I.

14

15 Table I: Possible Resulting Capacitances

16	C4
17	C5
18	C6
19	C4 + C5
20	C4 + C6
21	C5 + C6
22	C4 + C5 + C6

23

24 In Table I, the sign "+" designates summation. In one
25 embodiment, capacitor C4 has a capacitance of 5 μF
26 (microFarads), capacitor C5 has a capacitance of 10 μF and
27 capacitor C6 has a capacitance of 20 μF . Thus, in such an
28 embodiment, the possible resulting capacitance is between 5

1 μF and 35 μF , inclusive. It is to be understood that
2 capacitor networks 204 and 206 have substantially the same
3 circuit configuration as capacitor network 202. In a
4 preferred embodiment, switch 207 is configured so that each
5 capacitor network 202, 204 and 206 exhibits substantially
6 the same capacitance. A user adjusts switch 207 so that
7 capacitor networks 202, 204 and 206 exhibit a particular
8 capacitance that corresponds to a particular voltage spike
9 test being performed on UUT 30.

10 Referring to FIG. 2, voltage synchronization circuit
11 25 further comprises switch 300 which has switch contacts
12 301, 302, 303, 304, 305 and 306. Voltage synchronization
13 circuit 25 further includes voltage transformer 310.
14 Voltage transformer 310 includes 440 V_{rms} inputs and 115 V_{rms}
15 inputs. Switch contacts 301 and 302 are connected to switch
16 contacts 140 and 141, respectively. Switch contacts 303 and
17 305 are connected to the 440 V_{rms} inputs of voltage
18 transformer 310. Transformer 310 steps 440 V_{rms} down to 115
19 V_{rms} such that it can be used for synchronization of VSG 20
20 when calibrator 10 is used with a 440 V_{rms} three-phase
21 electrical system. Transformer 310 outputs synchronization
22 signal 312 which is inputted into VSG 20. Switch contacts
23 304 and 306 bypass transformer 310 and feed the 115 V_{rms}
24 synchronization signal 312 directly into VSG 20.

1 VSG 20 includes high voltage and common outputs 316 and
2 318, respectively. High voltage output 316 is connected to
3 one end of resistor R7. Common output 318 is connected to
4 switch contact 190. VSG 20 outputs a voltage spike through
5 high voltage and common outputs 316 and 318, respectively.

6 Prior to conducting any test, the power requirements of
7 UUT 30 must be evaluated so as to enable power supply 50 to
8 be configured to provide the correct power. If UUT 30 is a
9 115 V_{rms} system, then switch 300 is configured so that switch
10 contacts 301 and 302 are connected to the 115 V_{rms} inputs of
11 transformer 310 via switch contacts 304 and 306. Power
12 supply 50 is then configured to provide a 115 V_{rms} output.
13 If UUT 30 is a 440 V_{rms} system, then switch 300 is configured
14 so that switch contacts 301 and 302 are connected to the 440
15 V_{rms} inputs of transformer 310 via switch contacts 303 and
16 305. For purposes of facilitating explanation and
17 understanding of the invention, the ensuing description is
18 in terms of switch 300 being configured for a 115 V_{rms} UUT.

19 There are several voltage spike tests that must be
20 performed on UUT 30 in order to accurately test the
21 survivability and compatibility of UUT 30. In a first test,
22 a predetermined voltage spike waveform is applied to phase A
23 voltage input 40 and ground input 46 of UUT 30. In order to
24 accomplish this first test, the predetermined voltage spike
25 waveform is applied across phase A voltage line 108 and

1 ground line 114. In a second test, a predetermined voltage
2 spike waveform is applied to phase B voltage input 42 and
3 ground input 46 of UUT 30. In order to accomplish this
4 second test, a predetermined voltage spike waveform is
5 applied across phase B voltage line 110 and ground line 114.
6 In a third test, a predetermined voltage spike waveform is
7 applied to phase C voltage input 44 and ground input 46 of
8 UUT 30. In order to accomplish this third test, a
9 predetermined voltage spike waveform is applied across phase
10 C voltage line 112 and ground line 114. The manner in which
11 these aforesaid tests are implemented is described in detail
12 in the ensuing description.

13 In order to apply a predetermined voltage spike
14 waveform across phase A voltage line 108 and ground line 114
15 to implement the first test, switch 130 is configured so
16 that each pair of switch contacts shown in each row of Table
17 II are electrically connected together.

18 TABLE II

140	142
141	145
150	151
160	161
170	171
180	181
190	191

1 Next, switch 207 is configured so that capacitor networks
2 202, 204 and 206 yield a particular capacitance that will
3 provide the desired voltage spike waveform characteristics.
4 As a result, contact 140 is connected to phase B voltage
5 line 110 via contact 142, and contact 141 is connected to
6 phase C voltage line 112 via contact 145. Thus, a voltage
7 signal taken between phase B and C voltage lines 110 and
8 112, respectively, functions as the source for the
9 synchronization signal and is fed to switches 130 and 300.
10 This synchronization signal is outputted from switch 300
11 (via transformer 310 for 440 V_{rms} systems) as signal 312
12 which is inputted into VSG 20. The high voltage output 316
13 of VSG 20 is connected to phase A voltage line 108 via
14 switch contacts 180 and 181. The common output 318 is
15 connected to the input of capacitor network 206 via switch
16 contacts 190 and 191. Thus, capacitor network 206 is
17 connected between common output 318 and ground line 114.
18 Capacitor network 204 is connected between phase B voltage
19 line 110, via contacts 160 and 161, and ground line 114.
20 Capacitor network 202 is connected between phase C voltage
21 line 112, via contacts 170 and 171, and ground line 114.
22 The capacitance exhibited by each capacitor network 202, 204
23 and 206 affects the waveform characteristics of the
24 resulting voltage spike outputted via high voltage and
25 common outputs 316 and 318, respectively. Thus, the

1 capacitance exhibited by each capacitive network 202, 204
2 and 206 introduces the proper impedance to produce the
3 desired waveform characteristics of the voltage spike
4 waveform that is inputted into the phase A voltage input 40
5 of UUT 30.

6 In order to apply a predetermined voltage spike
7 waveform across phase B voltage line 110 and ground line 114
8 to implement the second test, switch 130 is configured so
9 that each pair of switch contacts shown in each row of Table
10 III are electrically connected together.

11 TABLE III

140	143
141	146
150	152
160	162
170	172
180	182
190	192

12
13 Next, switch 207 is configured so that capacitor networks
14 202, 204 and 206 yield a particular capacitance that
15 provides the desired voltage spike waveform characteristics.
16 As a result, contact 140 is connected to phase C voltage
17 line 112, via contact 143, and contact 141 is connected to
18 phase A voltage line 108, via contact 146. Thus, a voltage

1 signal taken between phase A and C voltage lines 108 and
2 112, respectively, functions as the source for the
3 synchronization signal and is fed to switches 130 and 300.
4 This synchronization signal is outputted from switch 300
5 (via transformer 310 for 440 V_{rms} systems) as signal 312
6 which is inputted into VSG 20. The high voltage output 316
7 of VSG 20 is connected to phase B voltage line 110 via
8 switch contacts 180 and 182. The common output 318 is
9 connected to the input of capacitor network 204 via switch
10 contacts 190 and 192. Thus, capacitor network 204 is
11 connected between common output 318 and ground line 114.
12 Capacitor network 202 is connected between phase C voltage
13 line 112, via contacts 170 and 172, and ground line 114.
14 Capacitor network 206 is connected between phase A voltage
15 line 108, via contacts 150 and 152, and ground line 114.
16 The capacitance exhibited by capacitor networks 202, 204 and
17 206 affect the waveform characteristics of the resulting
18 voltage spike outputted via high voltage and common outputs
19 316 and 318, respectively. Thus, the capacitance exhibited
20 by each capacitive network 202, 204 and 206 introduces the
21 proper impedance to produce the desired waveform
22 characteristics of the voltage spike waveform that is
23 inputted into the phase B voltage input 42 of UUT 30.

24 In order to apply a predetermined voltage spike
25 waveform across phase C voltage line 112 and ground line 114

1 to implement the third test, switch 130 is configured so
2 that each pair of switch contacts shown in each row of Table
3 IV are electrically connected together.

4 TABLE IV

140	144
141	147
150	153
160	163
170	173
180	183
190	193

5
6 Next, switch 207 is configured so that capacitor networks
7 202, 204 and 206 yield a particular capacitance that
8 provides the desired voltage spike waveform characteristics.
9 As a result, contact 140 is connected to phase A voltage
10 line 108, via contact 144, and contact 141 is connected to
11 phase B voltage line 110, via contact 147. Thus, a voltage
12 signal taken between phase A and B voltage lines 108 and
13 110, respectively, functions as the source for the
14 synchronization signal and is fed to switches 130 and 300.
15 This synchronization signal is outputted from switch 300
16 (via transformer 310 for 440 V_{rms} systems) as signal 312
17 which is inputted into VSG 20. The high voltage output 316
18 of VSG 20 is connected to phase C voltage line 112 via

1 switch contacts 180 and 183. The common output 318 is
2 connected to the input of capacitor network 202 via switch
3 contacts 190 and 193. Thus, capacitor network 202 is
4 connected between common output 318 and ground line 114.
5 Capacitor network 204 is connected between phase B voltage
6 line 110, via contacts 160 and 163, and ground line 114.
7 Capacitor network 206 is connected between phase A voltage
8 line 108, via contacts 150 and 153, and ground line 114.
9 The capacitance exhibited by capacitor networks 202, 204 and
10 206 affect the waveform characteristics of the resulting
11 voltage spike outputted via high voltage and common outputs
12 316 and 318, respectively. Thus, the capacitance exhibited
13 by each capacitive network 202, 204 and 206 introduces the
14 proper impedance to produce the desired waveform
15 characteristics of the voltage spike waveform that is
16 inputted into the phase C voltage input 44 of UUT 30.

17 As a result of the particular switching configuration
18 of switch 130, when the predetermined voltage spike waveform
19 is applied to one of the phase A, B or C voltage lines, the
20 voltage across the other two phase voltage lines is minimal
21 and cannot cause stress or damage to VSG 20.

22 Referring to FIG. 2, calibrator 10 further includes a
23 monitoring circuit that comprises resistors R8 and R9,
24 capacitor C7 and test ports 350 and 352. Resistors R8 and
25 R9 are configured in a voltage divider circuit. Capacitor

1 C7 filters out any high frequency components. Test ports
2 350 and 352 allow for the measurement of the line-to-ground
3 voltage V_{LG} . In one embodiment, resistors R8 and R9 have
4 resistances of about 99 K Ω and 1 K Ω , respectively, and
5 capacitor C7 has a capacitance of about 27 pF.

6 The present invention provides a technique for testing
7 the compatibility and survivability of three-phase
8 electrical devices which is relatively more safe and
9 efficient than prior art techniques. The present invention
10 allows for one test set up for all required test conditions
11 while the UUT is energized and also allows for the changing
12 of test instrumentation while the UUT is energized. As a
13 result, the present invention significantly reduces test
14 set-up and reconfiguration time. The present invention
15 allows for variation of the phase in which the voltage spike
16 is induced. This phase variation can be performed while UUT
17 30 is energized. It is not necessary to de-energize, rewire
18 circuitry, and then re-energize UUT 30 in order to adjust
19 the phase in which the voltage spike is induced. Additional
20 important advantages of the present invention is that it can
21 be easily transported and integrated with the other devices
22 and test equipment, and realized with commercially available
23 electrical components.

24 The principles, preferred embodiments and modes of
25 operation of the present invention have been described in

1 the foregoing specification. The invention which is
2 intended to be protected herein should not, however, be
3 construed as limited to the particular forms disclosed, as
4 these are to be regarded as illustrative rather than
5 restrictive. Variations in changes may be made by those
6 skilled in the art without departing from the spirit of the
7 invention. Accordingly, the foregoing detailed description
8 should be considered exemplary in nature and not limited to
9 the scope and spirit of the invention as set forth in the
10 attached claims.